CLAIMS

What is claimed is:

1. A method for stacked register aliasing in data hazard detection of a processor, comprising the steps of:

calling for a first group of registers within a register file of the processor;

detecting data hazards, if any, associated with first register identifiers of the first group;

calling for a second group of registers within the register file; and

detecting data hazards, if any, associated with second register identifiers of the second group, wherein the first and second register identifiers overlap in hazard detect logic across two or more rows of the register file.

2. A method of claim 1, the steps of calling comprising calling for a group within a 128-register register file.

3. A method of claim 2, the steps of mapping comprising detecting comprises utilizing groups of 32 register identifiers to alias data hazard detect logic to windows of 32-register frames

4. A processor for processing program instructions, comprising:

a register file;

an execution unit having an array of pipelines for processing the instructions and for writing bypass data to the register file; and

data hazard detect logic for detecting and aliasing data hazard detection for two or more rows of the register file

5. A system of claim 4, further comprising a register ID file for facilitating data hazard detection associated with rows of the register file, the register ID file having a plurality of register identifiers, the data hazard detect logic aliasing data hazard detection according to mapping of the register identifiers.

6. A system of claim 5, the register ID file mapping sequential 32-registers with the common hazard logic to more than 32 stacked registers of the register file to alias in 32-register sequences.

7. In data hazard detect logic of a processor of the type having a register file and a register ID file providing row-to-row data hazard detection, the improvement wherein the register file ID aliases row-to-row hazard detection of the register file by common data hazard detection logic for two or more rows of the register file.